REMARKS

Claims 1, 2 and 4 - 20 are pending in the present application, of which claims 15-20 have been withdrawn from consideration. By this Amendment, claim 1 has been amended. No new matter has been added. It is respectfully submitted that this Amendment is fully responsive to the Office Action dated May 19, 2005.

35 U.S.C. §112, Second Paragraph Rejection:

Claim 1 stand rejected under 35 U.S.C. §112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

This rejection is respectfully traversed.

Claim 1 has been amended to overcome this rejection. More specifically, claim 1, as amended, now calls for *a capacitor formed on or above said support substrate comprising a lower electrode having a first wide area and a first cut-away portion, a dielectric film covering the first wide area, and an upper electrode having a second wide area and a second cut-away portion, the first and second wide areas facing via the dielectric film to establish a capacitance*. For example, referring to Fig. 1G, the specification, page 9, lines 15-17 describes that the capacitor electrode comprises a first portion 20a having a wide area and a cut-away portion and a second portion 20b within the cut-away portion. The upper electrode is similarly patterned as shown in Fig. 1I.

In addition, claim 1 has also been amended to recite *wiring layer formed on or above said support substrate, leading some of said through holes filled with conductor upwards via one of said wide areas and one of said cut-away portions of said capacitor, having branches above said upper electrode to form wires of a second uniform pitch narrower than said first uniform pitch* For example, Cu wiring 25 is formed above the upper electrode as shown in Fig. 1K. There are three kinds of Cu wires: 1) those connected to the lower electrode, 2) those connected to the upper electrode, and 3) those not connected to either electrode. In addition, for example, semiconductor elements have wirings of a narrow pitch, while a circuit board has wirings of a wider pitch. Thus, the wirings adapted to the through holes in the support substrate is divided (branched) above the capacitor to form wirings of the narrow pitch as shown in Fig. 1T.

Accordingly, withdrawal of this rejection is respectfully requested.

As to the Merits:

As to the merits of this case, the Examiner relies on the newly cited reference of Gnadinger (U.S. Patent No. 5,229,647) in setting forth the following rejections:

1) claims 1, 4-6, 8-10, 13 and 14 stand rejected under 35 USC 103(a) as unpatentable over Yamauchi et al. (U.S. Patent No. 6,503,778) in view of Gnadinger;

2) claim 2 stands rejected under stand rejected under 35 USC 103(a) as unpatentable over Yamauchi et al. and Gnadinger in view of Malladi (U.S. Patent No. 5,939,782);

3) claim 7 stands rejected under 35 USC 103(a) as unpatentable over Yamauchi et al. and Gnadinger in view of Kabumoto et al. (U.S. Patent No. 5,883,428); and

4) claims 11 and 12 under 35 USC 103(a) as unpatentable over Yamauchi et al. and Gnadinger in view of Cuchiaro et al. (U.S. Patent No. 5,888,585).

Each of these rejections is respectfully traversed.

Yamauchi does not teach a support substrate made of a semiconductor substrate, as the Examiner admits. Further, Yamauchi only recites that the device layers 20, 40 may be applicable to capacitors (column 18), and does not teach any particular capacitor structures. That is, capacitor electrodes having wide areas and cut-away portions are not taught by Yamauchi. Yamauchi does not particularly show any capacitor nor the support substrate.

In other words, Yamauchi fails to disclose or fairly suggest the features of claim 1 concerning *a support substrate made of a semiconductor substrate having through holes filled with conductor in conformity with a first uniform pitch, a capacitor formed on or above said support substrate comprising a lower electrode having a first wide area and a first cut-away portion, a dielectric film covering the first wide area, and an upper electrode having a second wide area and a second cut-away portion, the first and second wide areas facing via the dielectric film to establish a capacitance.*

The wirings in Yamauchi have branches, but the pitch of the wirings is narrower just above the semiconductor substrate and becomes wider far above the substrate (see Fig. 9B). In other words, Yamauchi also fails to disclose or fairly suggest the features of claim 1 concerning *wiring layer formed on or above said support substrate, leading some of said through holes filled with conductor upwards via one of said wide areas and one of said cut-away portions of said capacitor, having branches above said upper electrode to form wires of a second uniform pitch narrower than said first uniform pitch.*

In order to compensate for the above-noted drawbacks and deficiencies of Yamauchi, the Examiner relies on the teachings of the secondary reference of Gnadinger. More specifically, the Examiner assets that "Gnadinger teaches (Fig. 4, col. 3, lines 37-57) the use of a semiconductor wafer (10) as a support in the structure of forming an interconnect structure."[1]

However, column 3, lines 37-57 of Gnadinger merely describes that through conductors are formed through the wafers and the abstract describes that a solid state memory unit is constructed using stacked wafers containing a large number of memory units. In other words, it is submitted that Gnadinger fails to provide any description or suggestion that any of the wafers is used as a support substrate.

Moreover, Gnadinger also fails to disclose any particular capacitor structures. As such, it is submitted that Yamauchi and Gnadinger, singly or in combination, fail to disclose or fairly suggest

[1] Please see, lines 16-17, page 3 of the Action.

the features as now set forth in claim 1 concerning *a support substrate made of a semiconductor substrate having through holes filled with conductor in conformity with a first uniform pitch, a capacitor formed on or above said support substrate comprising a lower electrode having a first wide area and a first cut-away portion, a dielectric film covering the first wide area, and an upper electrode having a second wide area and a second cut-away portion, the first and second wide areas facing via the dielectric film to establish a capacitance, wiring layer formed on or above said support substrate, leading some of said through holes filled with conductor upwards via one of said wide areas and one of said cut-away portions of said capacitor, having branches above said upper electrode to form wires of a second uniform pitch narrower than said first uniform pitch, and plural semiconductor elements disposed on or above said wiring layer, having terminals in conformity with the second uniform pitch, and connected with said wiring layer via said terminals.*

In view of the aforementioned amendments and accompanying remarks, the claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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